HR001118S0020
Millimeter-Wave Digital Arrays (MIDAS)
Frequently Asked Questions (FAQ)
February 12, 2018

Q1: Will there be multiple awards?

A1: Yes, multiple awards are expected (page 4 of BAA).

Q2: Will there be any downselects during the program?

A2: There are no formal downselects under this program. DARPA plans to evaluate the technical progress against the program metrics and make program decision based on the available funding. Among the metrics, the element pitch and power consumption are the major goals to be assessed to achieve the multi-beam, scalable, element-level digital array program objective.

Q3: Do you really want digital beamforming?

A3: Yes, as stated in the BAA for TA1/TA2, the use of analog beamforming techniques that eliminate spatial degrees of freedom at the sub-array level will be considered non-responsive to this BAA (page 7 of BAA). Alternative approaches in TA3 are acceptable if technically compelling.

Q4: May proposal submissions be classified?

A4: In general, it is expected that the hardware work under this program will be unclassified. However, if you feel your proposal would be stronger as a classified submission or contain a classified appendix, this is acceptable and Section IV.B.3.b of the BAA (Page 29-31) describes the procedure for classified submissions. If any aspect of your response is classified, please contact us as soon as possible at the BAA mailbox (HR001118S0020@darpa.mil) to start a conversation with the MTO Program Security Officer (PSO) to make proper arrangements. Do NOT submit any classified information through DARPA's BAAT proposal submission system.

Q5: Is DARPA planning to organize a multi-project wafer run?

A5: Proposers should budget for purchasing their own MPW/wafer runs and not count on a government organized MPW. If after performers are selected, the government sees an opportunity for cost sharing by purchasing a dedicated run, this may be done.

Q6: Can universities work on TA1 or TA2?

A6: Yes, if the university is willing to accept 6.3 funding and perform non-fundamental research.

Q7: Are universities allowed to accept 6.3 funding?

A7: Yes. However, this is university dependent; some universities will not accept 6.3 funding due to publication restrictions, so check with your office of sponsored research.

Q8: Is there any limit on the number of proposals an academic team can submit to TA-3? Is there a limit on the number of collaborations in TA1 or TA1/TA2 that an academic institution can be involved with?

A8: There is no limit to the number of proposals that a principle investigator may submit to a technical area; however, it is highly encouraged to submit your single best idea. There is no limit to the number of teaming arrangements for TA1 and TA1/TA2. Note that TA1/TA2 funding is 6.3 funding.

Q9: Is there any guidance for the size of a TA3 team?

A9: DARPA does not have a preconceived TA3 team size. A TA3 team should be sized in the appropriate manner to accomplish the proposed statement of work. The available funding for TA3 is stated in the BAA (page 4) and there will be multiple awards.

Q10: Do TA3 proposals also have to be at 18-50 GHz or should they be higher?

A10: TA3 work may be in the 18-50 GHz band or other wideband high frequency ranges. As described in page 14, “a successful proposal will describe the substantial innovation in the context of the broader goals of the program and clearly identify an aspect of the TA1/TA2 metrics that will be the focus of the proposed TA3 work.”

Q11: Would proposals for low-profile aperture development only be considered in TA3? Would a proposer in TA3 be introduced to proposers in TA1 and TA2 for teaming?

A11: It is expected that aperture development will be part of a TA1/TA2 joint proposal. An aperture ONLY proposal will only be considered in TA3. DARPA will not provide introductions for teaming purposes.

Q12: Can you provide more detail on the required program demonstrations (benchtop, anechoic chamber, flight test, etc.)?

A12: It is up to the proposers to outline compelling multi-beam demonstrations as the hardware development progresses throughout the program. Some combination of benchtop, anechoic and/or outdoor test range would be acceptable. A flight test that requires platform integration, government test assets or government test ranges is not expected. Also as part of the Deliverables, “sufficient documentation and support for testing at a government lab (AFRL, etc.) is expected” (page 15).

Q13: Does the program only address communications applications? Would a proposal that addresses more than one application be preferred?

A13: There are many applications of interest. However, the focus of the program is on the array hardware. The proposer defined demonstration should propose the intended application or applications.

Q14: What is the reasoning behind the 10 dBm IIP3 metric in TA1 and why is there no IIP3 metric for the TA2 receiver?

A14: The assumption is that linearity will be dominated by 3rd order intermodulation distortion performance because any random spurious nonlinearities will decorrelate across the array during beamforming, hence it is most relevant to specify an IIP3 referenced to the receiver input rather than an SFDR at the output of an ADC. The specific number is chosen such that when cascaded with the gain of an LNA in TA2, it can be calculated that the resulting system IIP3 will be around -5 dBm in phase 1 depending on the TA1 noise performance and choice of TA2 LNA gain and linearity. This will result in approximately 50 dB of SFDR in phase 1 for a 2-tone test at -30 dBm and approximately 60 dB of SFDR at the end of phase 2. No IIP3 is specified in TA2 because it directly falls out of the cascade analysis from the TA1 performance and the choice of TA2 LNA gain/linearity.

Q15: Is there a metric for the grating lobes?

A15: There should be no grating lobes within the specified scan range.

Q16: How much can performance be degraded at a 70 degrees scan angle?

A16: Scan loss should strive to be as close to cosine(theta) as possible.

Q17: Is the 3.2 GHz beam-bandwidth product metric for horizontal and vertical total, or horizontal and vertical for a total of 6.4 GHz?

A17: See Table 1, Note 9 in the BAA (page 11). One example calculation provided is 16 beams at 200 MHz in phase 2. If 32 linear polarized beams were produced, they

would only be able to support 100 MHz each which is within the 3.2 GHz beam-bandwidth product.

Q18: Is the incoming signal expected to have a 2 GHz bandwidth?

A18: The specifications are provided for the hardware and not the incoming signal. The instantaneous bandwidth requirement listed in Table 1 of the BAA and is ≥200 MHz in Phase 1 and ≥2 GHz in Phase 2.

Q19: Is there a definition for the digital interface?

A19: The digital interface is performer defined.

Q20: Is calibration power consumption or beamforming DSP power consumption included in power per channel metric?

A20: If the calibration is power cycled, then it should not be included in the calculation of the power consumption metric. Any DSP that runs continuously should be included in the metric calculation. As stated in Table 1, Note 10, if the tile is designed to support 16 elements or 32 channels, then the power per channel is the total power of the tile divided by 32.

Q21: In a multibeam system, inter-beam scrambling is going to be a problem. A peak to null ratio requirement would solve many problems.

A21: The BAA specifies linearity and noise performance for the hardware, which for specific waveforms and power levels, will limit the null depth through a beamforming calculation and is therefore not specified separately.

Q22: Will there be digital processing for phase shifting and summation at the tile level?

A22: As stated in the BAA, Table 1, Note 9 (Page 11), “Beamforming strategies will be left to performers to propose. Some strategies may warrant DSP hardware intimately integrated within transceivers in the tile building block, while other strategies may be best addressed with package level DSP implemented under TA2 after data is moved off of the tile.”

Q23: Since the instantaneous bandwidth is only 10% do you expect a tunable solution to be acceptable? Is there a requirement on the tuning speed?

A23: Wideband or tunable solutions are both acceptable. No tuning speed is specified.

Q24: Does a single tile need to run at multiple frequencies at the same time?

A24: A single tile is only required to run at one frequency at time.

Q25: Are there requirements or restrictions on waveforms, constellations, peak-to-average power ratios or power back-off?

A25: No waveforms or waveform metrics are specified.

Q26: Is the power density defined per channel or per polarization?

A26: The power density is defined per unit area and must meet the requirement when radiating linear polarization. If radiating circular polarization, the radiated power density will be approximately 3 dB higher.

Q27: How is the TA2 transmitter power amplifier efficiency defined, PAE, drain efficiency, etc? Should it be measured at max power or max efficiency? Is there a requirement for efficiency at power back-off?

A27: Assume that the TA2 power amplifier efficiency is defined by power-added efficiency (PAE) and that it should be measured at the maximum power. Striving to maintain efficiency at power back-off is important for some modern waveforms, but is not explicitly specified or required.

Q28: Does the TA2 power amplifier efficiency metric include the loss of the T/R switch or antenna/feed efficiency?

A28: While the loss of the T/R switch and any antenna feed loss is important to overall system efficiency, it is not necessary to include it in the efficiency measurement of the TA2 power amplifier. The goal of specifying the wideband efficiency performance in TA2 is to strive for innovative power amplifier solutions that achieve efficiency over wide bandwidth.

Q29: Is the 150 mW power metric in TA1, Phase 1, for the receiver (Rx) and transmitter (Tx), or the maximum of the Rx, Tx?

A29: Both the receiver and the transmitter need to be below the 150 mW power consumption metric in Phase 1. See Note 10 to Table 1 in the BAA (page 11).

Q30: Is the power consumption of any required SERDES included in the 150 mW power metric?

A30: Yes, the power metric includes any power consumed by SERDES, but amortized across the channels in a tile. See Note 10 to Table 1 in the BAA (page 11).

Q31: Does the power budget include the power associated with the thermal solution?

A31: No, the power metric does not include any active cooling power, however it is expected that passive cooling should be sufficient.